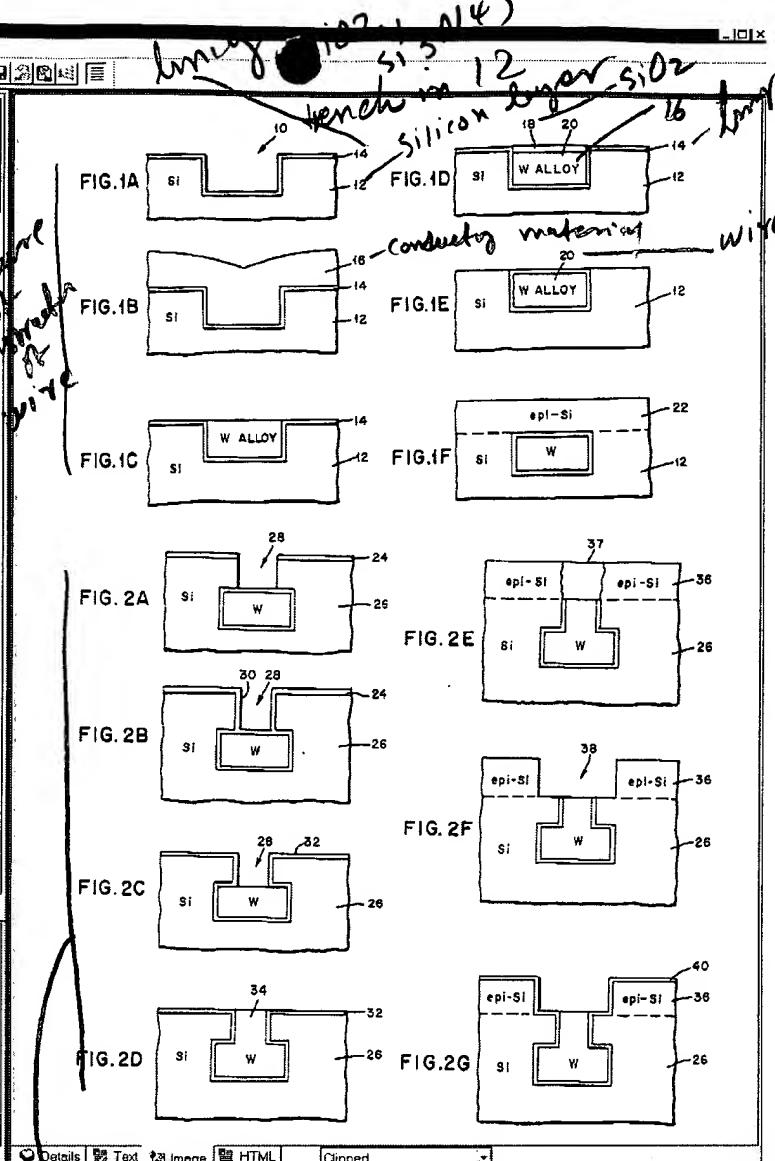


TDB-ACC-NO: NB8908403
 DISCLOSURE TITLE: Single-Crystal Silicon Embedded With Insulated Conducting Wires
 PUBLICATION-DATA: IBM Technical Disclosure Bulletin, August 1989, US
 VOLUME NUMBER: 32
 ISSUE NUMBER: 3B
 PAGE NUMBER: 403 - 407
 PUBLICATION-DATE: August 1, 1989 (19890801)
 CROSS REFERENCE: 0018-8689-32-3B-403
 DISCLOSURE TEXT:
 In packaging technology, a generic problem is that the packaging materials tend to have a different thermal expansion coefficient from that of silicon. Consequently, upon thermal cycling during operation a shear stress is exerted on those solder balls that join the chip and module, and fatigue failure of the balls occurs.
 This problem limits the size of the chip since the magnitude of the shear depends on the chip size. In order to overcome this problem so that a large chip can be used in VLSI, there has been a long term effort to develop ceramics which have the same thermal expansion.

Document ID	Kind Codes	Source	Issue Date	Pages
1	JP 2001223249	JPO	20010817	9
2	JP 2001144150	JPO	20010525	9
3	JP 10162613 A	JPO	19980619	8
4	JP 09237826 A	JPO	19970909	8
5	JP 01179353 A	JPO	19890717	4
6	EP 628644 A2	EPO	19941214	24
NB8908403	[REDACTED]	IBM TDB	19890801	1



Page 7

1 TDB-ACC-NO: NB8908403

DISCLOSURE TITLE: Single-Crystal Silicon Embedded With
Insulated Conducting

5 Wires

PUBLICATION-DATA: IBM Technical Disclosure Bulletin,
August 1989, US

10 VOLUME NUMBER: 32

ISSUE NUMBER: 3B

PAGE NUMBER: 403 - 407

15 PUBLICACION-DATE: August 1, 1989 (19890801)

CROSS REFERENCE: 0018-8689-32-3B-403

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30 join the chip and module, and fatigue failure of the
balls occurs.

This problem limits the size of the chip since the
magnitude of the

shear depends on the chip size. [In order to overcome

35 this problem so]

[that a large chip can be used in VLSI, there has been a]
long term)

[effort to develop ceramics which have the same thermal]
[expansion]

40 [coefficient as that of silicon. However, the material]
[which has the]

[best match of expansion coefficient with silicon is]
[silicon itself.]

- [In order to use silicon as a packaging]

45 [material, it must be]

possible to lay conducting wires and vias within it), same as with the multi-layered ceramic (MLC) substrates used today.) To achieve this,

5 a method is described to construct a three-dimensional network of

insulated conducting lines within a single-crystal silicon. The

10 procedure for the construction of a wire is illustrated in Figs. 1A -

1F, and of a via in Figs. 2A - 2G. ***** SEE ORIGINAL DOCUMENT *****

Wire Construction

A line trench 10 is first etched in silicon layer

15 Fig. 1A

shows the trench 10 (the cross-section of a line) having a lining 14 comprised of SiO₂/Si₃N₄/SiO₂

20 Fig. 1B shows the conformal deposition of a conducting material

16, such as W containing about 5 at .% of Si, or W-Si₂ containing

about 5 at .% excess Si.

25 Fig. 1C shows planarization of the surface by chemical and

mechanical polishing and etching away the excess W alloy or silicide.

Fig. 1D shows oxidation of the W alloy or silicide to produce a

30 thick layer 18 of SiO₂ on top of the line 20. Because SiO₂ is

thermodynamically more stable than the oxides of W, it will form on

35 the surface of the line. The composition of Si in the W alloy or

silicide [line 20] is chosen so that a thick SiO₂ layer 18 can grow on the wire surface.

40 Fig. 1E shows that by chemical etching, the oxide and nitride

on the Si surface are removed. Because the oxide 18 on the line is

thick, a layer of SiO₂ will survive the etching and insulate [wire 20].

45 Fig. 1F shows that by epi-Si and SOI (Si on Insulator) growth,

a Si layer 22 can be grown on the wire in a single

1 crystal Si
environment.

2 This procedure can be repeated to produce a]
3 second layer of

4 wires. Nevertheless, vias or through-holes are needed
5 between them
6 for interconnection.)

7 Via Construction: Fig. 2A shows the growth or
8 deposit of a

9 thick thermal SiO₂ layer 24 on the surface of Si layer
10 26. By

11 lithographic patterning, via hole 28 is opened in the
12 oxide by

13 etching, after which reactive ion etching is used to
14 drill a via in

15 the Si 26. Drilling stops at the bottom oxide surface
16 of the via.

17 Fig. 2B shows the growth of a sidewall oxide 30 on the
18 via. Some

19 oxide growth will occur simultaneously on the surface
20 as well as on

21 the bottom via surface. Fig. 2C shows that by reactive
22 ion etching

23 (RIE) the oxide on the bottom surface of the via can be
24 removed. This

25 etching will remove an equal thickness of the oxide on
the top

26 surface. Since it is thicker, a layer 32 of oxide
27 remains on the top

28 surface after etching. Due to the directional effect of
29 RIE, the

30 sidewall oxide of the via will not be etched away. In.
Fig. 2D, the

31 via is filled by selective deposition of W (or WSi₂),
i.e., the W

32 grows only on the W (or WSi₂) surface but not on the
SiO₂ surface,

33 resulting in a via surface 34 that is planar with its
surrounding. In

34 Fig. 2E, the oxide on the Si surface is etched away and
an epi-Si

35 layer 36 is grown over Si layer 26. At the same time,
silicide and

36 poly-Si region 37 will grow over the via. The epi-Si
37 has a

38 thickness the same as the wire thickness.

39 - Fig. 2F shows that when a line trench 38 is

etched over the

via, the silicide and poly-Si 37 over the via are removed. The poly-

Si can be etched selectively to form an extended via

5 hole by using an

etchant which attacks epi-Si and poly-Si at different rates. Fig. 2G

10 shows that a lining 40 of SiO₂/Si₃N₄/iO₂ is formed on the second

trench. Laser etching or RIE is used to remove the very thin oxide

just over the via before filling the second level trench with W alloy

15 or silicide again. W or WSi₂ can be used as conducting materials in this process.

Other conductors also can be used, but they must have a melting

20 point higher than the processing temperatures involved. For example,

Al is not good since its melting point is lower than that (1050°C)

used to grow epi-Si. Also, the conductor must be stable with SiO₂

25 which is the isolating material used here. For example, Ti is not a

good choice since it decomposes SiO₂ upon annealing above 400°C. For

30 the same reason, when a Ti-Si alloy is oxidized, it is the oxide of

Ti rather than SiO₂ that will form preferentially on the surface.

Therefore, only certain transition metals, such as W, Mo, Pt, Co,

35 etc., can be used. Transition metal silicides and noble metals, such as Au and Cu containing a few percent of excess Si, are generally suitable.

40 Thermal stress in the line upon heating and cooling must be addressed. From this viewpoint, the best conducting line in Si is

45 made of heavily doped poly-Si, provided that its conductivity is good

enough for general purpose application. The stress problem is handled

by adding a few percent of Si into the metal conductor, such as W.

The Si is needed to form SiO_2 on the line surface for isolation.

5 - When Si atoms diffuse to the surface to form an oxide,

vacancies diffuse back into the metal (or silicide) to form voids.

10 - These voids will cushion the stress in the line, in particular the

compression stress which is more serious since it may crack the oxide

coating. Another technique to reduce the stress effect is to unfill

15 - a small part of the trench during deposition by making use of the

shadow of the trench wall. The unfilled part again provides a

cushion space for stress relief.

20 - In planarizing the via, selective W deposition has been used.

It is a simple and available technique. On the other hand, this

technique has not been developed for other metals.

25 Nevertheless, in

filling a via the procedure of filling a trench, as has been

disclosed here, can be followed.

30 An important question about high density packing of conducting

lines is how to achieve effective heat dissipation].

Since cooling of

[a chip is necessary, one side of a Si wafer can be used to build]

35 [active devices and the other side (the back side) of the wafer can

be used for packaging purposes.] In fact, wafers can be stacked one

40 on top of the other and joined by solder joints. For packaging

purposes, the quality of the epitaxial Si layer is not as critical as

that in the active side. In other words, some polycrystalline Si

45 grains in the epi-Si layer are tolerable.

- In device applications, for example, in a multi-layer SOI

technology, a random-access memory chip can be built in such a way

that peripheral circuits are located over the cell array to save the

5 chip area (*). In such applications both vertical and horizontal

wires in between two silicon layers are needed for interconnections.

10 The method disclosed here for making insulated wires in single-crystal Si is useful in multi-layer SOI technology.

15 Reference: * C. L. Cohen, "LSI in 3-D Coming Soon,"
Electronics Week, 16-17 (April 8, 1985).

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30 COPYRIGHT STATEMENT: The text of this article is Copyrighted (c) IBM Corporation 1989. All rights reserved.

PURPOSE: To improve mass productivity and reliability by forming a conductive path composed of the simple substance or complex of an interstitial nitride into a ceramic substrate obtained by sintering aluminum nitride and onto the surface of a sintered body.

CONSTITUTION: TiN paste in which polyvinyl butyral as a binding agent and isopropyl alcohol as a solvent are added to titanium nitride (TiN) is prepared. The molded form 5 of aluminum nitride (AlN) is formed, and conductive paths 2a, 2b are printed onto the surface of the molded form 5 by the TiN paste and dried. A molded form 6 in which $Y<SB>2</SB>O<SB>3</SB>$ is added to AlN as a sintering assistant is shaped, and a plurality of conductive holes 6a are worked and the molded form 6 is superposed. Conductive paths 3a, 3b are printed by using the TiN paste, and dried. The whole is compressed in the thickness direction and unified, degreasing treatment is executed, and the whole is baked in a nitrogen atmosphere, thus acquiring a substrate, which is bonded firmly with a ceramic substrate, has the conductive paths having excellent oxidation resistance and has superior mass productivity and high reliability.

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[Details](#) [Text](#) [Image](#) [HTML](#) [Full](#)

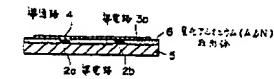
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2 JP 04233187 A		JPO	19920821	1	CER
3 JP 04233186 A		JPO	19920821	1	CER
JP 02082641 A		JPO	19900323	3	CER
5 JP 02082598 A		JPO	19900323	4	MANI
6 JP 01230295 A		JPO	19890913		MANI
7 JP 01230294 A		JPO	19890913		MANI

[Details](#) [Text](#) [Image](#) [HTML](#) [Full](#)

特許平2-82841(3)
第 1 図
図示する如きは本発明で使用した電子ペーパー
ストの印刷パターンおよびAlNの成形体の構造
を、第2図は本発明によるセラミック多層基板の
平面図、第3図は本発明および発明例の対象とな
るセラミック多層基板の断面図である。

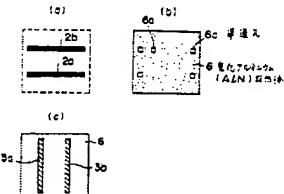
- 1 … マトリック基板、2a, 2b, 3a,
- 3b … 基電極、4 … 線道部、5, 6
- … 室化アルミニウム成形体、6a …

導通孔

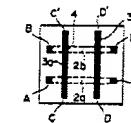


第 2 図

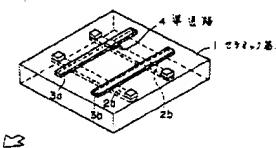
特許出願人 下條西日本株式会社
大 旗 入 事 業 所



第 3 図



第 4 図



-231-

4月27日
09/6/1993

ABSTRACT:

PURPOSE: To improve mass-productivity, realize complete coupling with a sintered Si₃N₄ board and improve reliability by a method wherein layers of mixture of AlN, zirconium oxide and organic material and layers of mixture of AlN and organic material are alternately printed a plurality of times on the sintered Si₃N₄ board and baked.

CONSTITUTION: Layers of insulator material and layers converted into conductor by the reaction at the time of baking are alternately printed a plurality of times on a sintered silicon nitride ceramic board 7 and baked. The insulator material printed on the surface of the ceramic board is composed of mixture of aluminum nitride and organic material. The material converted into conductor by the reaction at the time of baking is composed of a mixture of aluminum nitride, zirconium oxide and organic material. When the mixing ratio of aluminum nitride and zirconium oxide in the mixture of aluminum nitride, zirconium oxide and organic material is expressed by $(\text{AlN})_x(\text{ZrO}_2)_{1-x}$, zirconium nitride enough to provide a conductivity is made of the mixture having the composition $(x)=0.2-0.9$.

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Details Text Image HTML Full

Document ID	Kind Codes	Source	Issue Date	Pages
1 JP 08306483 A		JPO	19961122	6 [COO]
2 JP 04233187 A		JPO	19920821	1 CER
3 JP 04233186 A		JPO	19920821	1 CER
4 JP 02082641 A		JPO	19900323	3 CER
5 JP 02082598 A		JPO	19900323	14 MAN
6 JP 01230295 A		JPO	19890913	MAN
7 JP 01230294 A		JPO	19890913	MAN

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特許平2-82598 (3)
本発明が示す焼成する焼成は焼成と同時に生成してお
り、射出ペーストA層とガスプロセスペーストA層
との結合性も充分で、完全に一体化していた。
また、この焼成後124、125、126および127を
構成する焼成はセラミックスであるため、耐久性
が高く、耐候性においても焼成中で印字して、8
時間の焼成を行っても性能は認められなかった。

なお、本発明では、2種類のペーストAおよび
Bを用いた時の組合せとしてガソリニカルテラ
ルを用いたが、他の組合せにおいてもよく、また、
組合せはイソシアヌルアクリコールを用いたが、他の
溶剤を用いてもよい。

また、(a)の前記組合せとして焼化ジルコニウム
を構成したが、他の可溶性の導電助剤を併せても、
また組入なくても本発明が有効であることは確
わりない。

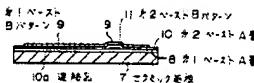
一方、焼成後124、125、126および127を構
成する焼成が生成するA1とB1の組合せ反応は、
モル比でA1: B1=3:1で起こる。従って、
A1: B1=3:1の組合せ配合した混合物を塗

4. 施工の簡単な説明

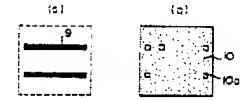
第1圖は本発明によるセラミック多層基板の施
工例、第2圖は本発明によるセラミック多層基板
における各層の印刷パターンを示す平面図、第3
圖は本発明の一實施例によるセラミック多層基板
の断面図を示す平面図、第4圖は焼成の焼成方法
によるセラミック多層基板の断面図である。

- (a) 第1ペーストAパターン
- (b) 第2ペーストAパターン
- (c) 第3ペーストAパターン
- (d) 第4ペーストAパターン

第 1 図



第 2 図



-541-

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US-CL-CURRENT: 264/680,427/96 ,428/901

JP 01-230295 (4)

ABSTRACT:

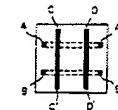
PURPOSE: To improve mass productivity, and obtain high reliability, by performing baking after a plurality of layers of material turning to conductor by reaction at the time of baking, and a plurality of layers of material being insulator are alternately printed on a sintered body of silicon nitride.

CONSTITUTION: On a sintered body 11 of silicon nitride, paste A12 is screen-printed on the whole surface, and dried at 150°C. After drying, thereon, paste B13 is screen-printed in a pattern as shown by (a), and dried in the same manner. After drying, thereon, paste A14 is screen-printed in a pattern as shown by (b), and dried in the same manner. After this laminated body is degreased, baking is performed at 1800°C for two hours in a nitrogen atmosphere. The silicon nitride ceramic multilayer board obtained in this manner has a perfectly high conductivity in the printed part of paste B after baking. Since the material constituting a conducting channel is ceramics, the durability is high, and the oxidation resistance is large.

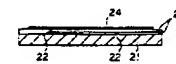
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第 3 図



第 4 図



	Document ID	Kind Codes	Source	Issue Date	Pages	
1	JP 08306483 A		JPO	19961122	6	COO
2	JP 04233187 A		JPO	19920821	1	CER
3	JP 04233186 A		JPO	19920821	1	CER
4	JP 02082641 A		JPO	19900323	3	CER
5	JP 02082598 A		JPO	19900323	4	MAN
6	JP 01230295 A		JPO	19890913	14	MAN
7	JP 01230294 A		JPO	19890913		MAN
8						

-570-

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12



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L12: [349] 10 and vacuum | US 6365242 B1 | Tag: S | Doc: 86/349...



U.S. Patent Apr. 1, 2003 Sheet 4 of 4 US 6,364,196 B1

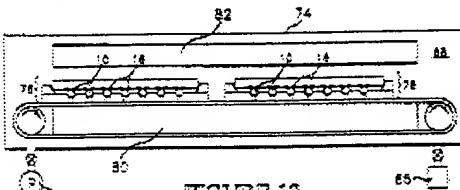


FIGURE 12

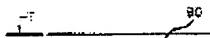


FIGURE 13A

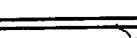


FIGURE 15A



FIGURE 13B



FIGURE 15B



FIGURE 13C

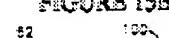


FIGURE 15C



FIGURE 13D

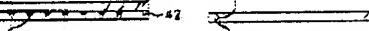


FIGURE 15D



FIGURE 14A



FIGURE 14B

>> claim comprising a photosensitive glass suitable wet etchant comprises HF. In addition, photosensitive glasses and etchants are commercially available from Dow Corning under the trademark "FOTOFORM".

(35) The diameter D2 (FIG. 5A) and depth D (FIG. 5A) of the ball retaining cavities 44 will be dependent on the size of etch openings 94 in the etch mask 92 and on the etch parameters. At the same time that the ball retaining cavities 44 are etched, the previously machined ~~vacuum~~ conduits 46 can also be etched. As shown in FIG. 14A, ~~vacuum~~ conduits 46 formed by laser machining will initially be circular in cross section. As shown in FIG. 14B, following an anisotropic wet etch with a silicon wafer blank 90, the ~~vacuum~~ conduits will have a multi faceted cross section (e.g., six sided).

(36) Following the etch procedure, the etch mask 92 can be stripped using a suitable wet chemical. For an etch mask 92 comprising Si_{sub}.3 N_{sub}.4 one suitable wet chemical for stripping the mask 92 comprises H_{sub}.3 PO_{sub}.4.

(37) Next, as shown in FIG. 13D, the substrate alignment member 50 can be attached to the ball retaining plate 42. One method of attachment is by forming an adhesive layer 96 out of silicone.



Courier New



12



B



I



U



I



B



S



A



C



D



E



U



I



B



S



A



C



D



E



U



I



B

L14: (20) 13 AND (439/... | US 6416332 B1 | Tag: S | Doc: 4/20 | Full

Eric J. Jakola, both of Kansas, all of
(CA)

Signer: Nortel Networks Limited, St. Laurent,
(CA)

Notice: Subject to any disclaimer, the term of this
patent is extended or adjusted under 35
U.S.C. 154(b) by 0 days.

PL. No.: 09/739,896

DA: Dec. 20, 2000

CL: H01R 12/00
Int. CL: 439/70; 439/331
Id. of Search: 439/68, 70, 71,
439/330, 331

References Cited

U.S. PATENT DOCUMENTS

969 A • 12/1977 Dean

6,313,235 A 3/21/00 Lee et al.
6,075,235 A 6/20/00 Liao et al.

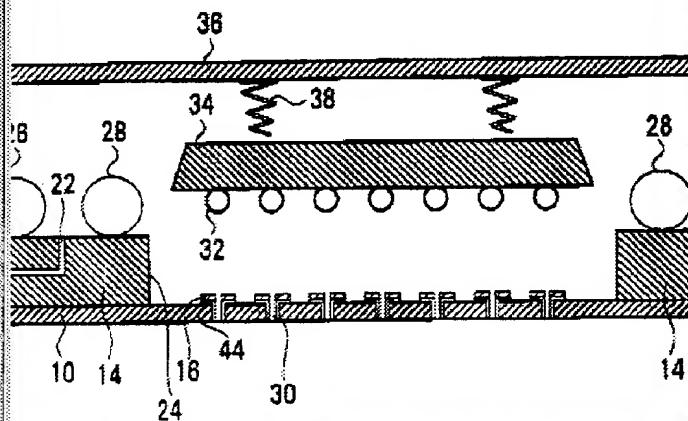
* cited by examiner

Primary Examiner—Khiem Nguyen
(57)

ABSTRACT

The present invention relates to a socket, in particular, high speed ICs in BGA packages holding an IC package in the test socket. Resilient conductive test pads positioned in array to match an array of spherical contacts of a BGA package. The BGA package is held by the use of holes centered on the spherical contacts and sealed. The test pads have two flexible seals on the top of the substrate to enclose the test pads. The flexible seals, surface of a support and a socket lid, cavity to which a vacuum is applied. Thereby compressed pulling the socket, thus the IC package leads into contact with the test pads.

25 Claims, 2 Drawing S

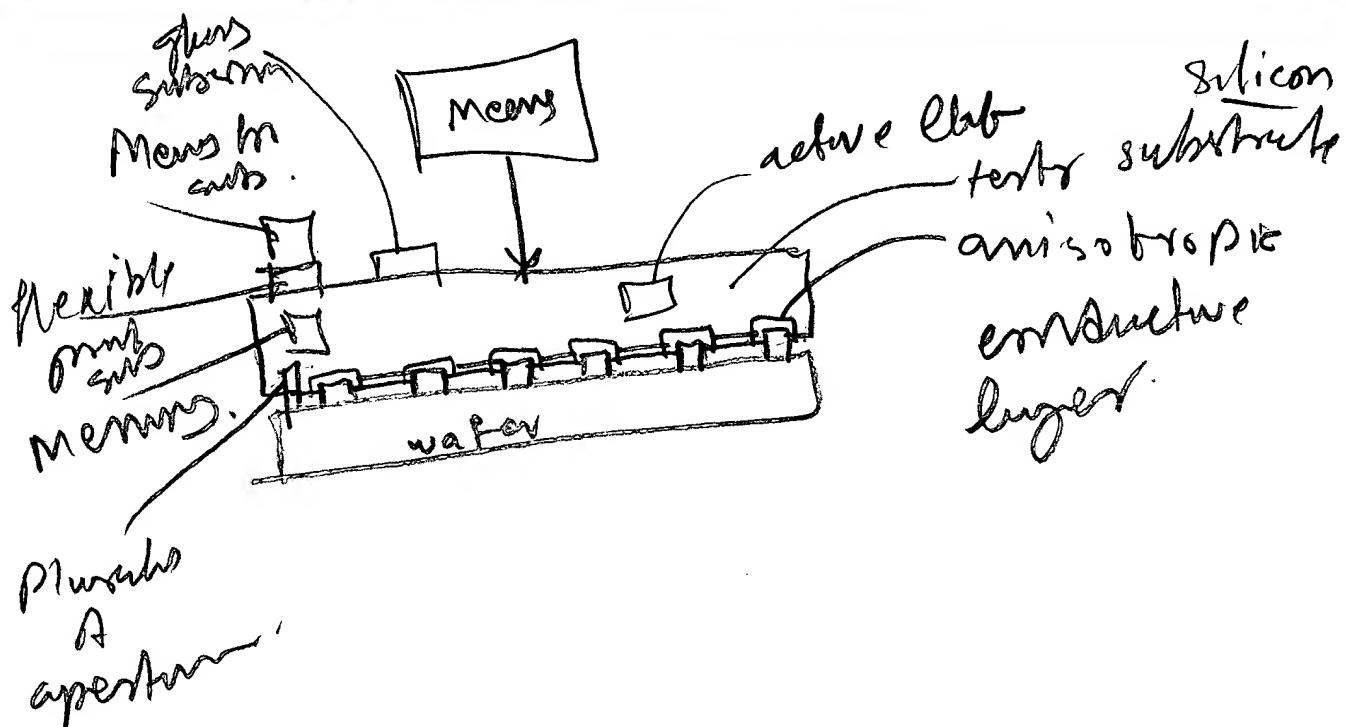


square opening 24 defined in it. The opening 24 surrounds a plurality of conductive test pads 16 on the top surface of the substrate 10. The conductive test pads 16 are comprised of a resilient conductive material which will deform when subject to compressive force and then return to its former shape when the compressive force is removed. An example of such a material is an electrically conductive elastomer which may be screen printed onto the surface of the substrate 10 prior to assembly of the support 14 to the substrate 10 and is typically in the range of 0.25 millimeters to 0.50 millimeters in thickness. Other possible materials include polycarbonates and conductive thermoplastic compounds. Preferably, the material from which conductive test pads 16 are constructed may be removed and replaced when it is damaged avoiding the need to replace the entire substrate 10. The conductive test pads 16 depicted in FIG. 1 are circular in shape however, other geometries of conductive test pads 16, such as square shaped pads, may be used.

(7) The conductive test pads 16 have holes 30 through their centers, preferably extending through both conductive test pads 16 and substrate 10. The holes 30 may or may not be conductively plated within the substrate 10. Between the conductive test pads 16 and the

Details Text Image HTML Full

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US-PAT-NO: 4385434

DOCUMENT-IDENTIFIER: US 4385434 A

TITLE: Alignment system

----- KWIC -----

Detailed Description Text - DETX (24):

Further, although mechanical drives have been illustrated, any other type of drive mechanism may be used. For example, a truss structure 80 may be formed in platen 12c, FIG. 10, having a plurality of beams 82 running in both directions across the bottom of platen 12c separated by holes or bays 84, as shown in FIG. 11. Heat, which may be applied for example by a heat source 86 consisting of a laser beam, may be used to strike selected ones of beams 82 to cause them to expand and deform selected zones on the platen and wafer. The truss structure 80 with bays 84 separating trusses 82 helps to confine the thermal energy paths along the trusses to enable a measure of directionality and control to be exercised over the thermal expansion. Alternatively, heating and cooling may be applied by heaters or Peltier devices applied to or embedded in the truss structure 80c, such as in FIG. 11, wherein heaters 88 are attached directly to trusses 82.

[Details](#) [Text](#) [Image](#) [HTML](#) KWIC

	Document ID	Kind Codes	Source	Issue Date	Pages	
29	US 5401359 A		USPAT	19950328	8	Dry
30	US 5269146 A		USPAT	19931214	7	The
31	US 5231291 A		USPAT	19930727		Wafer
32	US 5227862 A		USPAT	19930713		Pro
33	US 5220171 A		USPAT	19930615		Wafer
34	US 5193347 A		USPAT	19930316		Hea
35	US 4385434 A		USPAT	19830531	10	All

[Details](#) [Text](#) [Image](#) [HTML](#)

United States Patent (19)

Zehnpfennig et al.

4,385,434

May 31, 1983

[54] ALIGNMENT SYSTEM

[75] Inventor: Theodore F. Zehnpfennig, Weyland; Giuseppe Aurilia, Arlington, both of Mass.

[73] Assignee: Vizidyne, Inc., Burlington, Mass.

[21] Appl. No.: 371,786

[22] Filed: Jun. 4, 1981

[51] Int. Cl.: A61K 27/02; H01L 7/00

[52] U.S. Cl.: 29/575 R; 250/492 A

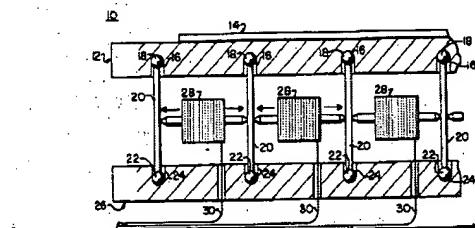
[54] Field of Search: 29/575 R; 576 R; 250/492 A

[56] References Cited

U.S. PATENT DOCUMENTS

3,875,416 4/1975 Sparer 29/577 X

20 Claims, 11 Drawing Figures



[Details](#) [Text](#) [Image](#) [HTML](#) Full

fr
09/673953

portion of the heat produced as a result of the X-ray irradiation is diffused over the X-Y plane. Consequently, a heat flow of a heat flow density of about 1000 W/m² impinges on the heat receiving side (Peltier device 104 side) of the heat pipe 105.

Detailed Description Text - DETX (47):

Like the third embodiment, also with the structure of the present embodiment it is possible to reduce the displacement of the attracting block 101 to be caused as a result of the exposure operation. Further, since it is sufficient that the temperature sensor 119 is provided between the wafer and the Peltier device 304, in the present embodiment it may be provided on the heat pipe 305.

Detailed Description Text - DETX (51):

In a portion of the outside surface of a first constituent element 402.sub.1, a wafer attracting surface 401 is formed. In a portion of the outside surface of a third constituent element 402.sub.3, a Peltier device 404 is mounted. In the present embodiment, the bottom face of the wafer attracting surface 401 of the first constituent element 402.sub.1 provides a heat receiving surface, while

Details Text Image HTML KWIC

	Document ID	Kind Codes	Source	Issue Date	Pages	
29	US 5401359 A		USPAT	19950328	8	Dry
30	US 5269146 A		USPAT	19931214	7	The
31	US 5231291 A		USPAT	19930727		Waf
32	US 5227862 A		USPAT	19930713		Pro
33	US 5220171 A		USPAT	19930615	27	Wafer
34	US 5193347 A		USPAT	19930316	12	Hel
35	IIS 4385434 A		USPAT	19830531	10	All

Details Text Image HTML

U.S. Patent June 16, 1993 Sheet 7 of 15 5,220,171

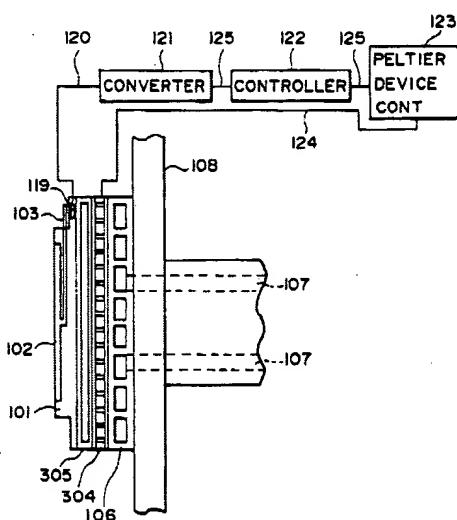


FIG. 7

US-PAT-NO: 5231291

DOCUMENT-IDENTIFIER: US 5231291 A

TITLE: Wafer table and exposure apparatus with the same

----- KWIC -----

Detailed Description Text - DETX (2):

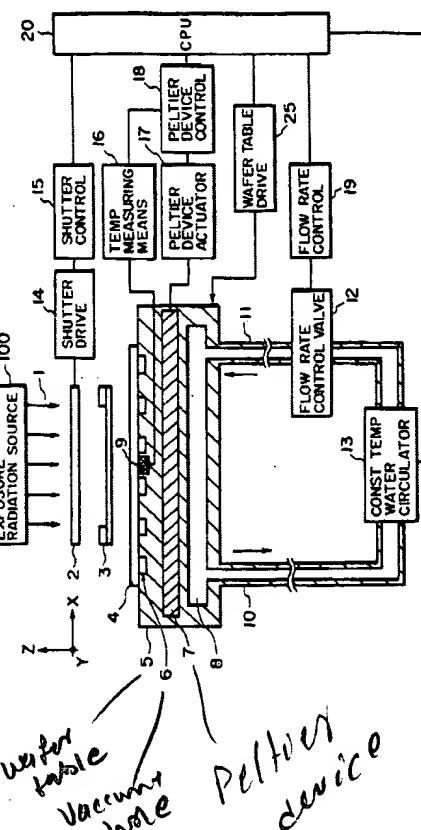
FIG. 1 schematically illustrates a step-and-repeat type exposure apparatus with a wafer table, according to an embodiment of the present invention. In FIG. 1, denoted at 1 is exposure radiation energy such as light or X-rays, for example, supplied from an exposure radiation source 100; at 2 is a shutter for defining a desired exposure time; at 3 is a mask and at 4 is a wafer. The mask 3 and the wafer 4 are opposed to each other and are substantially parallel to an X-Y plane, with a small gap maintained therebetween. The irradiation of the mask 3 and the wafer 4 with the exposure radiation energy 1 is controlled by opening/closing the shutter 2. Denoted at 5 is a wafer table for holding the wafer 4 thereon. The wafer table is provided with vacuum grooves 6 for holding by vacuum the wafer 4 on its wafer holding surface, a Peltier device 7 effective to transmit the thermal energy produced inside the wafer table by the exposure radiation rays 1 to a constant temperature water bath 8.

	Document ID	Kind Codes	Source	Issue Date	Pages	
29	US 5401359 A		USPAT	19950328	8	Dry
30	US 5269146 A		USPAT	19931214	7	The
31	US 5231291 A		USPAT	19930727	12	Wafer
32	US 5227862 A		USPAT	19930713	79	Pro
33	US 5220171 A		USPAT	19930615	27	Wafer
34	US 5193347 A		USPAT	19930316	12	He
35	US 4385434 A		USPAT	19830531	10	All

Details Text Image HTML

KWIC

U.S. Patent July 27, 1993 Sheet 1 of 4 5,231,291



wafer table
vacuum hole
Peltier device

FIG. 1

US-PAT-NO: 6215545

DOCUMENT-IDENTIFIER: US 6215545 B1

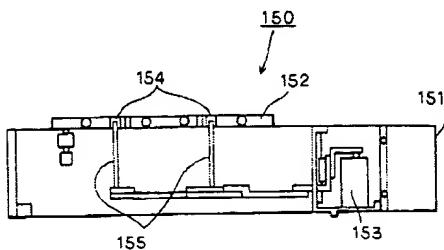
TITLE: Substrate processing apparatus

----- KWIC -----

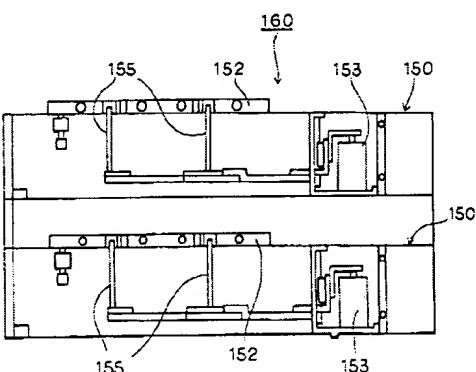
Detailed Description Text - DETX (33):

In the example shown in FIG. 7, a wafer W is cooled by water whose temperature is kept constant, the water being circulated in a circulation path (not shown) of the cooling table 152. Alternatively, the cooling table 152 may have a Peltier device so as to cool the wafer W.

U.S. Patent Apr. 10, 2001 Sheet 7 of 8 US 6,215,545 B1



F I G . 7



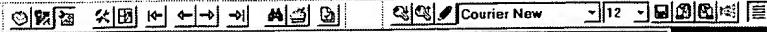
F I G . 8

Details Text Image HTML KWC

	Document ID	Kind Codes	Source	Issue Date	Pages	
24	US 6215545 B1		USPAT	20010410	17	Sub
25	US 6094268 A		USPAT	20000725	74	Pro
26	US RE36242 E		USPAT	19990629	13	Heli
27	US 5894341 A		USPAT	19990413	29	Exp
28	US 5714791 A		USPAT	19980203	9	On
29	US 5401359 A		USPAT	19950328	8	Dry
30	US 5269146 A		USPAT	19931214	7	The
31	US 5144621 A		USPAT	19920721	10	Ther

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12:24 PM



US-PAT-NO: 6215545

DOCUMENT-IDENTIFIER: US 6215545 B1

TITLE: Substrate processing apparatus

----- KWIC -----

Detailed Description Text - DETX (33):

In the example shown in FIG. 7, a wafer W is cooled by water whose temperature is kept constant, the water being circulated in a circulation path (not shown) of the cooling table 152. Alternatively, the cooling table 152 may have a Peltier device so as to cool the wafer W.

[Details](#) [Text](#) [Image](#) [HTML](#) [KWIC](#)

	Document ID	Kind Codes	Source	Issue Date	Pages	
24	US 6215545 B1		USPAT	20010410	17	Sub:
25	US 6094268 A		USPAT	20000725	74	Pro:
26	US RE36242 E		USPAT	19990629	13	Hei:
27	US 5894341 A		USPAT	19990413	129	Exp:
28	US 5714791 A		USPAT	19980203	9	On:
29	US 5401359 A		USPAT	19950328	8	Dry:
30	US 5269146 A		USPAT	19931214	7	The:
31						

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US6215545B1

(12) United States Patent
Matsuyama(10) Patent No.: US 6,215,545 B1
(44) Date of Patent: Apr. 10, 2001

(54) SUBSTRATE PROCESSING APPARATUS

5,972,110 * 10/1599 Akimoto 118-52

FOREIGN PATENT DOCUMENTS

10-144763 3/1998 (JP).

* cited by examiner

Primary Examiner—Russell Adams

Assistant Examiner—Hung Henry Nguyen

(74) Attorney, Agent, or Firm—Rader, Fishman & Gruber

(37) ABSTRACT

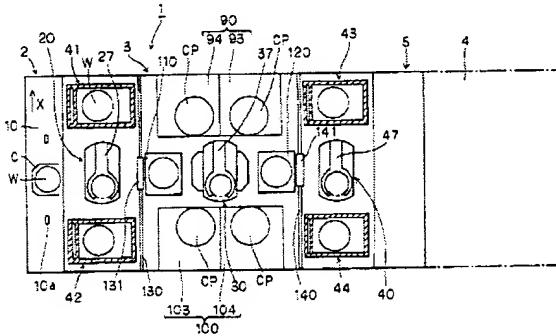
A has: conveying unit, a second conveying unit, and a third conveying unit, each of which conveys a wafer, are disposed in parallel in a wafer processing unit. A first heat treatment unit group and a second heat treatment unit group are oppositely disposed with respect to the second conveying unit. A third heat treatment unit group and a fourth heat treatment unit group are oppositely disposed with respect to the third conveying unit. A developing process unit group and a resist coating unit group are oppositely disposed with respect to the second conveying unit. A first transferring table is disposed between the first conveying unit and the second conveying unit. A second transferring table is disposed between the second conveying unit and the third conveying unit. Since the second conveying unit conveys a wafer among the developing process unit group, the resist coating unit group, and each transferring table, thermal variation of the film thickness of a film of processing solution can be suppressed.

(56) References Cited

U.S. PATENT DOCUMENTS

5,664,254 * 9/1997 Okamura et al.	396,612
5,762,745 * 6/1998 Hirose	266,545
5,826,129 * 10/1998 Shieh et al.	398,611
5,876,280 * 3/1999 Kanno et al.	424,187

19 Claims, 8 Drawing Sheets





US-PAT-NO: 6332322

DOCUMENT-IDENTIFIER: US 6332322 B1

TITLE: Electronic device having a thermally isolated element

----- KWIC -----

Detailed Description Text - DETX (70):

The characteristics of the thin film-shaped Peltier device vary from chip to chip, from wafer to wafer, and from lot to lot. Therefore, the thin film-shaped Peltier device can be used when it is not required to very precisely control the temperature of the functional material 306 at a set value or when the amount of heat generated by the functional material does not vary greatly.

U.S. Patent Dec. 26, 2001 Sheet 4 of 10 US 6,332,322 B1

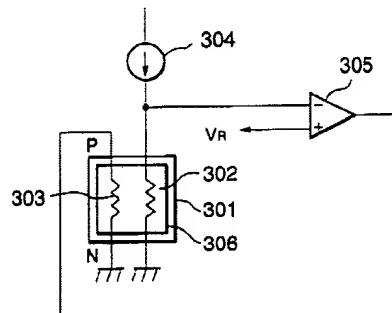


FIG. 4A

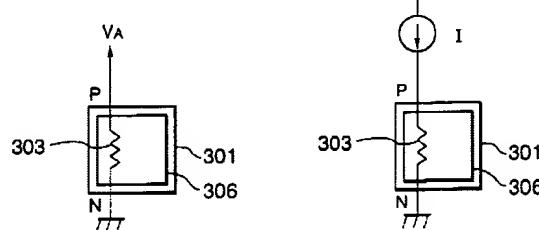


FIG. 4B

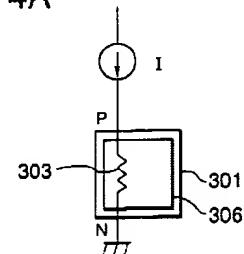


FIG. 4C

	Document ID	Kind Codes	Source	Issue Date	Pages	
23	US 6332322 B1		USPAT	20011225	21	Ele
24	US 6287435 B1		USPAT	20010911	29	Metl
25	US 6215545 B1		USPAT	20010410	17	Sub
26	US 6094268 A		USPAT	20000725	74	Pro
27	US RE36242 E		USPAT	19990629	13	Heli
28	US 5894341 A		USPAT	19990413	29	Exp
29	US 5714791 A		USPAT	19980203	9	On-

DOCUMENT-IDENTIFIER: US 20020158328 A1

TITLE: Ceramic substrate for semiconductor fabricating device

----- KWIC -----

Brief Description of Drawings - Table CWU - DRTL (1):

- 1 Explanation of Symbols 1, 11, 63 ceramic substrate 2, 22, 32a, 32b chuck
 positive electrostatic layer 3, 23, 33a, 33b chuck negative electrostatic layer 2a, 3a semicircular arc part 2b, 3b combteeth-shaped part 4 ceramic dielectric film 5, 12, 25, 61 resistance heating element 6, 13, 18 external terminal 7 metal wire 8 Peltier device 9 silicon wafer 10 ceramic heater 14 bottomed hole 15 through hole 16, 17, 19 conductor-filled through hole 20, 30, 101, 201, 301, 401 electrostatic chuck 25a metal covering layer 35, 36 blind hole 41 supporting case 42 coolant outlet 43 inhalation duct 44 coolant inlet 45 heat insulator 62 chuck top conductor layer 65 guard electrode 66 ground electrode 66a non-electrode formed area 67 groove 68 suction hole 501 wafer prober

[Details](#) [Text](#) [Image](#) [HTML](#) KWIC

Document ID	Kind Codes	Source	Issue Date	Pages
1 US 20020158328		US-PGPUB	20021031	28
2 US 20010002918		US-PGPUB	20010607	15
3 US 6507006 B1		USPAT	20030114	21
4 US 6464393 B2		USPAT	20021015	16

[Details](#) [Text](#) [Image](#) [HTML](#)

(19) United States

(21) Patent Application Publication (20) Pub. No.: US 2002/0158328 A1
 Hiramatsu et al.(22) Pub. Date: Oct. 31, 2002
 (24) CERAMIC SUBSTRATE FOR SEMICONDUCTOR FABRICATING DEVICE
 (52) U.S. Cl. 257/700

(76) Inventor: Yasuji Hiramatsu, Gifu (JP); Yasutaka Ito, Gifu (JP)

(57) ABSTRACT

The objective of the invention is to provide a ceramic substrate, wherein even if rapid temperature rising or rapid temperature falling occurs, no problem of warping or warpage of the ceramic substrate occurs, wherein, in case that the ceramic substrate is a ceramic substrate constituting an electrostatic chuck, local dispersion of chuck power is eliminated, in case that the ceramic substrate is a ceramic substrate constituting a hot plate, local dispersion of temperature of a wafer treating face is eliminated, in case that the ceramic substrate is a ceramic substrate constituting a wafer prober, dispersion of applied voltage of a guard electrode or a ground electrode is minimized so that a stray capacitor or noise can be reduced. The ceramic substrate of the invention is a ceramic substrate provided with a conductor layer on the surface of the ceramic substrate or inside the ceramic substrate, wherein the ratio (t_1/t_2) of the average thickness of the conductor layer (t_1) to the average thickness of the ceramic substrate (t_2) is less than 0.1 and; a dispersion of the thickness of the conductor layer is in a range of -70 to +150%.

(21) Appl. No.: 09/926,800

(22) PCT Filed: Apr. 18, 2001

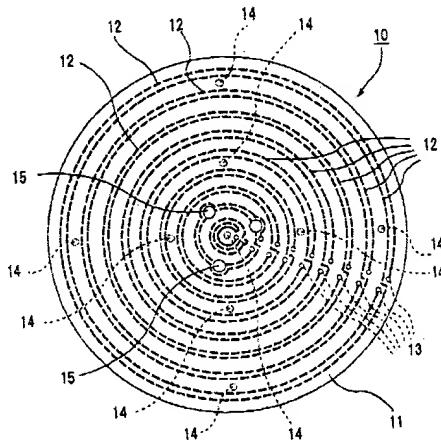
(24) PCT No.: PCT/JP01/03299

(30) Foreign Application Priority Data

Apr. 24, 2000 (JP) 2000-121936

Publication Classification

(51) Int. Cl.: H01L 23/053



Cannot use. because it don't

DOCUMENT-IDENTIFIER: US 20010002918 A1

TITLE: Surface temperature sensor head

----- KWIC -----

Summary of Invention Paragraph - BSTX (22):

[0020] This improvement contrives to reduce the temperature fluctuation induced by the touch of the probe needles by maintaining the probe at the same temperature as the wafer. For the purpose, this improvement provides the probe with a Peltier device and a temperature sensor. The Peltier device can heat or cool the probe by alternating the directions of current flow. The temperature sensor is a thermocouple. The tip of the thermocouple is buried into the probe for sensing exact temperature of the probe. The reason why the tip is buried into the probe is that exact temperature can be measured by reducing the heat resistance between the tip and the probe.

	Document ID	Kind Codes	Source	Issue Date	Pages	
1	US 20020158328		US-PGPUB	20021031	28	Ceram
	US 20010002918		US-PGPUB	20010607	15	Surf
3	US 6507006 B1		USPAT	20030114	21	Ceram
4	US 6464393 B2		USPAT	20021015	16	Surf

(19) United States

(12) Patent Application Publication

Tatoh



US 20010002918A1

(20) Pub. No.: US 2001/0002918 A1

(21) Pub. Date:

Jun. 7, 2001

(34) SURFACE TEMPERATURE SENSOR HEAD

Publication Classification

(75) Inventor: Nobuyoshi Tatoh, Hyogo (JP)

(51) Int. Cl. 7/04 H01L 35/02; G01K 7/04

(52) U.S. Cl. 374/199, 136/230

Correspondence Address:
MEDIMOTI, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20004-3096 (US)

(57) ABSTRACT

(73) Assignee: Sumitomo Electric Industries, Ltd.

09/725,502

(21) Appl. No. 09/725,502

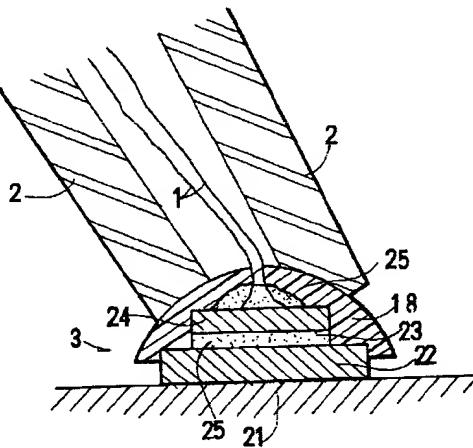
(22) Filed: Nov. 30, 2000

(30) Foreign Application Priority Data

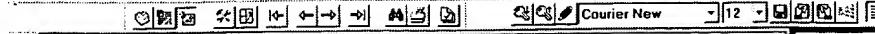
Dec. 3, 1999 (JP) 344569/1995

(57) ABSTRACT

A surface temperature sensor head including a first layer made of a material of a heat conductivity higher than 100 W/mK, a second layer having a crossing tips of a thermocouple and a braze material and a third layer made of a material of a heat conductivity higher than 100 W/mK, the braze material uniting the crossing tips, the first layer and the third layer. The sensor head enables a temperature probe to measure temperatures of an object non-destructively with high spatial resolution.



Can not use because of date.



US-PAT-NO: 6507006

DOCUMENT-IDENTIFIER: US 6507006 B1

TITLE: Ceramic substrate and process for producing the same

----- KWIC -----

Detailed Description Text - DETX (1):

EXPLANATION OF SYMBOLS 1, 11, 63 ceramic substrate 2, 22, 32a, 32b chuck positive electrode electrostatic layer 3, 23, 33a, 33b chuck negative electrode electrostatic layer 2a, 3a semicircular part 2b, 3b comb-teeth-shaped part 4 ceramic dielectric film 5, 12, 25, 61 resistance heating element 6, 13, 18 external terminal 7 metal line 8 Peltier device 9 silicon wafer 10 ceramic heater 14 bottomed hole 15 through hole 16, 17, 18 plated through hole 20, 30, 101, 201, 301, 401 electrostatic chuck 25a metal covering layer 35, 36 blind hole 41 supporting case 42 coolant outlet 43 inhalation duct 44 coolant inlet 45 heat insulator 62 chuck top conductor layer 65 guard electrode 66 ground electrode 66a non-electrode forming area 67 groove 68 suction hole 501 wafer prober

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	Document ID	Kind Codes	Source	Issue Date	Pages
1	US 20020158328		US-PPGPUB	20021031	28
2	US 200110002918		US-PPGPUB	20010607	15
3	US 6507006 B1		USPAT	20030114	21
4	US 6464393 B2		USPAT	20021015	16

KWIC

(12) United States Patent
Hiramatsu et al.(10) Patent No.: US 6,507,006 B1
(15) Date of Patent: Jan. 14, 2003

(54) CERAMIC SUBSTRATE AND PROCESS FOR PRODUCING THE SAME

(75) Inventor: Yasuji Hiramatsu, Gifu (JP); Yasutaka Ito, Gifu (JP)

(73) Assignee: Ibiden Co., Ltd., Ogaki (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/869,594

(22) PCT Filed: May 15, 2000

(66) PCT No.: PCT/JP00/03080

§ 371 (c)(1), (2), (4) Date: Aug. 9, 2001

(57) PCT Pub. No.: WO01/03972

PCT Pub. Date: Aug. 30, 2001

(30) Foreign Application Priority Data

Feb. 25, 2000 (JP) 2000-049482

(51) Int. Cl.⁷ H03F 3/68

(52) U.S. Cl. 219/144.1

(58) Field of Search 219/144.1, 460.1, 219/451.1, 455.1, 456.1, 467.1, 468.1, 533, 544, 546, 547, 548; 218/307, 338, 314, 119, 724, 725

(56) References Cited

U.S. PATENT DOCUMENTS

3,067,310 A * 12/1952 Wada et al. 219-541

4,024,207 A * 7/1977 Iwada et al. 219,504
4,443,691 A * 4/1984 Seiter 219,203
5,068,517 A * 11/1991 Tsuchi et al. 219,543
5,072,238 A * 12/1991 Iwada et al. 219,543
6,280,970 A * 6/2000 Yamada et al. 218,725
6,233,557 A * 10/2000 Kawahara et al. 219,544

FOREIGN PATENT DOCUMENTS

JP 62-167396 10/1987
JP 5-25274 2/1993
JP 8-273614 10/1996
JP 9-183567 7/1997
JP 2000-12194 1/2000

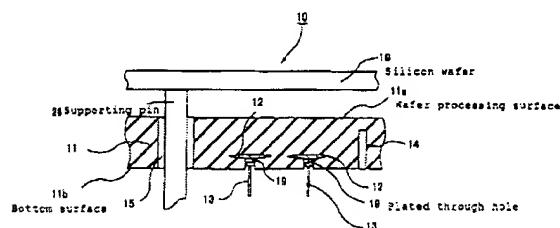
* cited by examiner

Primary Examiner—Sang Park
(74) Attorney, Agent, or Firm—Oblon, Spivak, McClelland,
Mayer & Neustadt, P.C.

(57) ABSTRACT

An object of the present invention is to provide a ceramic substrate that is superior in heat uniformity and thermal shock resistance, and has a large chuck power in the case that the ceramic substrate is made to be an electrostatic chuck. The ceramic substrate of the present invention is a ceramic substrate comprising a conductor layer formed therein, characterized in that a section of the edge of the conductor layer is in a peaked shape.

18 Claims, 8 Drawing Sheets



One inventor is common
Same assignee

KWIC

US-PAT-NO: 6464393
 DOCUMENT-IDENTIFIER: US 6464393 B2
 TITLE: Surface temperature sensor head
 ----- KWIC -----
Brief Summary Text - BSTX (22):
 This improvement contrives to reduce the temperature fluctuation induced by the touch of the probe needles by maintaining the probe at the same temperature as the wafer. For the purpose, this improvement provides the probe with a Peltier device and a temperature sensor. The Peltier device can heat or cool the probe by alternating the directions of current flow. The temperature sensor is a thermocouple. The tip of the thermocouple is buried into the probe for sensing exact temperature of the probe. The reason why the tip is buried into the probe is that exact temperature can be measured by reducing the heat resistance between the tip and the probe.

	Document ID	Kind Codes	Source	Issue Date	Pages
1	US 20020158328		US-PPGPUB	20021031	28
2	US 20010002918		US-PPGPUB	20010607	15
3	US 6507006 B1		USPAT	20030114	21
	US 6464393 B2		USPAT	20021015	16

(12) United States Patent
Tatoh(10) Patent No.: US 6,464,393 B2
(15) Date of Patent: Oct. 15, 2002

(54) SURFACE TEMPERATURE SENSOR HEAD

(75) Inventor: Nobuyoshi Tatoh, Hyogo (JP)

(73) Assignee: Sumitomo Electric Industries, Ltd., Osaka (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 23 days.

(21) Appl. No.: 09/725,502

(22) Filed: Nov. 30, 2000

(65) Prior Publication Data

(30) Foreign Application Priority Data

Dec. 3, 1999 (JP) 11-344569

(51) Int. Cl.: G01K 7/00

(52) U.S. Cl.: 314/119, 336.233

(58) Field of Search: 374/120, 179, 135/232, 233, 234.1

(56) References Cited

U.S. PATENT DOCUMENTS

2,846,620 A • 6/1968 Lindstrand 334/234.1

2,977,411 A • 1/1961 Bell et al. 136.233

4,755,438 A • 1/1988 Germanco et al. 374:179

4,685,922 A • 7/1987 Chao 374:31

US06464393B2

FOREIGN PATENT DOCUMENTS

DE 4223440 A1 • 10/1994 374:120

DE 4223453 A1 • 11/1994 374:120

JP 5204838A * 4/1977 374:179

JP 4-197,425 374:179

JP 4-200,045 374:179

JP 05116928 A * 15/1993 374:120

JP 7-74218 35/951

JP 11-122569 31/1999

* cited by examiner:

Primary Examiner—Diego Gutierrez

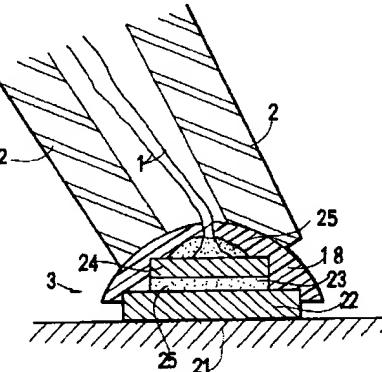
Assistant Examiner—Mirella Jagan

(74) Attorney, Agent, or Firm—McDermott, Will & Emery

ABSTRACT

A surface temperature sensor head including a first layer made of a material of a thermal conductivity higher than 100 W/mK, a second layer having a crossing tip of a thermocouple, a third layer carried on the second layer, and a third layer made of a material of a heat conductivity higher than 100 W/mK, the braiding material uniting the crossing tip, the first layer and the third layer. The sensor head enables a temperature probe to measure temperature of an object non-destructively with high spatial resolution.

20 Claims, 7 Drawing Sheets





US-PAT-NO: 6507006

DOCUMENT-IDENTIFIER: US 6507006 B1

TITLE: Ceramic substrate and process for producing the same

----- KWIC -----

Detailed Description Text - DETX (1):

EXPLANATION OF SYMBOLS 1, 11, 63 ceramic substrate 2, 22, 32a, 32b chuck positive electrode electrostatic layer 3, 23, 33a, 33b chuck negative electrode electrostatic layer 2a, 3a semicircular part 2b, 3b comb-teeth-shaped part 4 ceramic dielectric film 5, 12, 25, 61 resistance heating element 6, 13, 18 external terminal 7 metal line 8 Feltier device 9 silicon wafer 10 ceramic heater 14 bottomed hole 15 through hole 16, 17, 18 plated through hole 20, 30, 101, 201, 301, 401 electrostatic chuck 25a metal covering layer 35, 36 blind hole 41 supporting case 42 coolant outlet 43 inhalation duct 44 coolant inlet 45 heat insulator 62 chuck top conductor layer 65 guard electrode 66 ground electrode 66a non-electrode forming area 67 groove 68 suction hole 501 wafer prober

[Details](#) [Text](#) [Image](#) [HTML](#)

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	Document ID	Kind Codes	Source	Issue Date	Pages	
US	US 6507006 B1		USPAT	20030114	21	Cer
20	US 6464393 B2		USPAT	20021015	16	Sur
21	US 6399926 B2		USPAT	20020604	13	Hea
22	US 6332322 B1		USPAT	20011225	21	Elec
23	US 6287435 B1		USPAT	20010911	29	Metal
24	US 6215545 B1		USPAT	20010410	17	Sub
25	US 6094268 A		USPAT	20000725	74	Proc

[Details](#) [Text](#) [Image](#) [HTML](#)

KWC

(12) United States Patent
Hiramatsu et al.

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(54) CERAMIC SUBSTRATE AND PROCESS FOR PRODUCING THE SAME

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(52) U.S. Cl.: 219/61.1

(58) Field of Search: 219/61.1, 401, 451, 451.1, 455.1, 541, 544, 546, 547, 548, 338/307, 309, 314, 116/724, 725

(56) References Cited

U.S. PATENT DOCUMENTS

3,047,310 A * 12/1962 Welz et al. 219/541

FOREIGN PATENT DOCUMENTS

4,094,207 A * 3/29/77 Taneda et al. 219/524

4,443,981 A * 4/2/84 Saito 216/223

5,068,517 A * 11/5/91 Tsuyuki et al. 219/543

5,072,236 A * 12/1/91 Yamada et al. 219/543

5,083,786 A * 6/27/92 Yoshida et al. 116/725

5,131,557 A * 10/20/92 Kawashita et al. 219/544

* cited by examiner

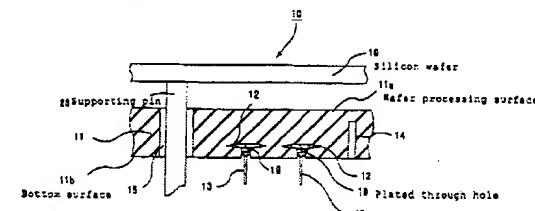
Primary Examiner—Sang Park

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(57) ABSTRACT

An object of the present invention is to provide a ceramic substrate that is superior in heat uniformity and thermal shock resistance, and has a large output power in the case that the ceramic substrate is used to be an electrode circuit or a certain substrate of the present invention. A ceramic substrate comprising a conductor layer formed thereto, characterized in that a section of the edge of the conductor layer is in a peaked shape.

18 Claims, 8 Drawing Sheets


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US-PAT-NO: 3037064

DOCUMENT-IDENTIFIER: US 3037064 A

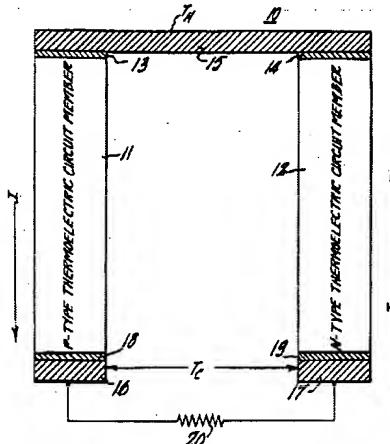
TITLE: Method and materials for obtaining low resistance bonds to thermoelectric bodies

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RE 3,037,064 U.S. Patent Office Patented May 29, 1962 2 the amount of Peltier cooling by as much as 25%. For the effect of contact resistance on maximum cooling obtained in Peltier devices, see FIG. 5 of "Evaluation and Properties of Materials for Thermoelectric Applications," by F. D. Rosi and E. G. Ramberg, in "Thermoelectricity," edited by P. H. Egli, John Wiley and Sons, Inc., New York, 1960. It is therefore an object of the instant invention to provide improved methods and materials for making low resistance electrical contacts to thermoelectric circuit members. Another object of the invention is to provide improved methods and materials for obtaining resistance, mechanically strong connections to thermoelectric components. A further object of

May 29, 1962 F. D. ROSI ET AL 3,037,064
METHOD AND MATERIALS FOR OBTAINING LOW RESISTANCE BONDS TO THERMOELECTRIC BODIES Filed Dec. 12, 1960



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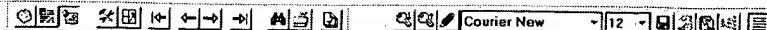
Document ID	Kind Codes	Source	Issue Date	Pages
21	US 3220198 A	USOCR	19651130	7
22	US 3192727 A	USOCR	19650706	5
23	US 3181304 A	USOCR	19650504	3
24	US 3075031 A	USOCR	19630122	6
25	US 3037065 A	USOCR	19620529	5
26	US 3037064 A	USOCR	19620529	4

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thermoelectric members, or the auxiliary components, or the electrical contacts to the two members, will reduce the efficiency of the device. Thermoelectric devices which utilize electrical energy for environmental cooling and refrigeration by means of the Peltier effect also include two thermoelectrically coupled Patented May 29, 1962 2 30 amperes at 0.1 volt. Accordingly, if any high resistance contacts are present, considerable Joulean heat will be dissipated, and the efficiency of the device will be decreased. The presence of high resistance contacts on the thermoelectric bodies has been a serious problem in the fabrication of both Seebeck and Peltier thermoelectric devices. High resistance contacts can reduce the cooling produced by Peltier devices as much as 40% below the theoretical maximum value. A contact resistance of only 10 1/4 of the sum of the resistance of the two thermoelements in a Peltier device can reduce the amount of Peltier cooling by as much as 25%. For a more complete discussion of the effect of contact resistance on maximum cooling obtained in Peltier devices, see chapter 8, "Evaluation and Properties of Materials for Thermoelectric Applications," by F. D. Rossi and E. G. Ramberg, in "Thermoelectricity," edited by P. H. Egli, John Wiley and Sons, Inc., New York, 1960. It is therefore an object of the instant invention to provide improved thermoelectric devices. Another object of the invention is to provide improved methods for

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Document ID	Kind Codes	Source	Issue Date	Pages	Links
20	US 3226804 A	USOCR	19660104	3	Metal
21	US 3220198 A	USOCR	19651130	7	The
22	US 3192727 A	USOCR	19650706	5	Iso
23	US 3181304 A	USOCR	19650504	3	Pel
24	US 3075031 A	USOCR	19630122	6	Lead
25	US 3037065 A	USOCR	19620529	5	Metal
26	US 3037064 A	USOCR	19620529	4	Metal

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May 29, 1962 E. F. HOCKINGS ET AL 3,037,065
METHOD AND MATERIALS FOR THERMOELECTRIC BODIES
Filed May 12, 1961

FIG. 1.

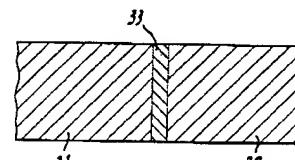
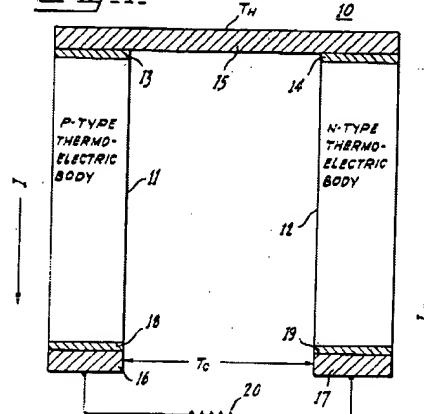


FIG. 2.

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